REMARKS

At the time of the Final Office Action dated October 18, 2002, claims 1-21 were pending in this application. Of those claims, claims 1-3, 11 and 13 have been rejected and claims 14-20 have been withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b). Applicants also acknowledge, with appreciation, the Examiner's allowance of claims 4-10, 12 and 21. Accordingly, the only remaining issue pivots about the patentability of claims 1-3, 11 and 13.

Claim 1 has been amended to clarify that the active regions partition the insulating film between adjacent resistor elements. Applicants submit that the present Amendment does not generate any new matter issue.

Claims 1-2, 11 and 13 are rejected under 35 U.S.C. § 102(b) for lack of novelty as evidenced by Babcock et al., U.S. P.G. Publication No. US 2002/0033519 A1 (hereinafter Babcock)

In the second enumerated paragraph of the Office Action, the Examiner asserted that Babcock discloses a semiconductor device corresponding to that claimed. This rejection is respectfully traversed.

On page two of the Office Action, the Examiner referred to Fig. 2C of Babcock and stated: "active regions are located to the left and the right of the STI." Furthermore, on page five of the Office Action, the Examiner stated: "[t]herefore, the active region is located beneath the

transistor gate structure, the active region being proximate to each of the resistor elements." In response, Applicants note claim 1 recites "active regions proximate to each of said resistor elements" (emphasis added). This limitation, however, is not identically described by Babcock within the meaning of 35 U.S.C. § 102. For example, *assuming arguendo* that active regions surround the transistor gate structure 80 in Fig. 2C, there is no active region proximate to the center trim resistor 60. The only features disclosed by Babcock that are proximate to the trim resistor 60 are an isolation structure 20 below the trim resistor 60 and a pair of isolation regions 110 on the sides of the trim resistor 20. Thus, there is no disclosure in Babcock that an active region is proximate to the trim resistor 60. As such, Babcock fails to identically describe the claimed limitation of active regions proximate to each of the resistor elements.

Claim 1 now clarifies that the active regions partition the insulating film between adjacent resistor elements. This feature is illustrated, for example, in Figs 1A and 1B of Applicants' disclosure, and described in page 9, lines 19-22. Babcock, however, fails to disclose or suggest this feature. The multiple resistors 60, 70 of Babcock are all formed on an isolation structure 20. Furthermore, there is no teaching within Babcock that active regions are formed between the resistors 60, 70 of Babcock or that the insulating film is partitioned by the active regions between adjacent resistor elements.

The above argued structural differences between the semiconductor device defined in independent claim 1 and Babcock's semiconductor device undermine the factual determination that Babcock identically describes the claimed invention within the meaning of 35 U.S.C. § 102. Applicants, therefore, respectfully submit that the imposed rejection of claim 1 under 35 U.S.C. §

102 for lack of novelty as evidenced by Babcock is not factually viable and, hence, solicit withdrawal thereof.

As claims 2, 11 and 13 depend ultimately from independent claim 1, Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 102 for lack of novelty as evidenced by Babcock. Thus, Applicants submit that claims 2, 11 and 13 are patentable over Babcock at least on the basis of their dependency upon claim 1. Applicants, therefore, respectfully solicit withdrawal of the rejections of claims 2, 11 and 13 under 35 U.S.C. § 102 for lack of novelty as evidenced by Babcock.

Claim 3 is rejected under 35 U.S.C. § 103 for obviousness predicated upon Babcock in view of Wolf

In the fourth enumerated paragraph of the statement of the rejection, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of Babcock in view of Wolf to arrive at the claimed invention. This rejection is respectfully traversed.

Claim 3 depends ultimately from independent claim 1, and Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 102 for lack of novelty as evidenced by Babcock. Specifically, Babcock neither discloses nor suggests active regions proximate to each of the resistor elements or active regions that partition the insulating film between adjacent resistor elements. The secondary reference to Wolf does not cure the argued deficiencies of Babcock because Wolf also does not teach active regions proximate

to each of the resistor elements or active regions between adjacent resistor elements. Accordingly, the proposed combination of references would not yield the claimed invention. Applicants, therefore, respectfully submit that the imposed rejection of claim 3 under 35 U.S.C. § 103 for obviousness predicated upon Babcock and Wolf is not factually or legally viable and, hence, solicit withdrawal thereof.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicants have made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicants invite the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicants hereby respectfully request reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

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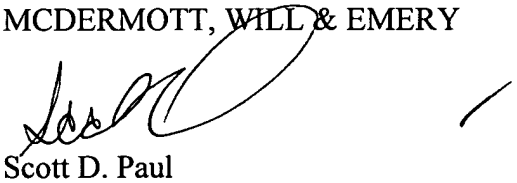

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Version with markings to show changes made

IN THE CLAIMS:

1. (Twice Amended) A semiconductor device having a plurality of resistor elements formed on an insulating film in predetermined regions on a surface of a semiconductor substrate, said semiconductor device comprising

active regions proximate to each of said resistor elements, wherein said active regions partition said insulating film between adjacent resistor elements.